

## Abstract

Proposed is a control unit featuring clocked data transmission between a processor ( $\mu\text{C}$ ) and at least one further circuit (ASIC 1, 2, n), the processor ( $\mu\text{C}$ ) itself outputting the clock pulse (SCKr). The processor ( $\mu\text{C}$ ) monitors the clock pulse (SCKr) based on the output signals of

5 at least two clock outputs (10, 11).

(Figure 1)